UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/491,810	01/28/2000	Thomas Justin Sullivan	10981801-1	9074

22879 7590 03/24/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	13

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/491,810	SULLIVAN, THOMAS JUSTIN	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 17 and 26 are objected to for containing the following informalities:

a. In claim 17, line 2, please change the limitation "and" to --an--.

b. In claim 26, line 3, please change the limitation "exception" to --exceptional-- .

3. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 20-25 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Roussel et al., US Patent 6,230,257, cited as a prior art reference in paper number 2, mailed on September 27, 2002.

6. Referring to claim 20, Roussel et al. have taught a method for performing single-instruction multiple-data instructions comprising:

a. applying a plurality of data values on an operand bus for two consecutive cycles (Figure 4A, column 4, lines 24-58);

b. latching a first data value in a multiply accumulate (MAC) unit during a first cycle (Figure 4A, column 4, lines 24-58);

c. initiating execution of the multiply and accumulate functions on the first data value and latching a second data value in the MAC unit during a second cycle (Figure 4A, column 4, lines 24-58);

d. deferring a first MAC unit result responsive to the first data value (Figure 4A, column 4, lines 24-58, element M3);

e. initiating execution of the multiply and accumulate functions on the second data value during a cycle subsequent to the second cycle to generate a second MAC unit result (Figure 4A, column 4, lines 24-58); and

f. generating a plurality of control signals responsive to the first data value, the second data value, and an exceptional condition when identified by tile MAC unit (column 6, lines 9-22).

7. Referring to claim 21, Roussel et al. have taught the method of claim 20, as described above, and further comprising applying the plurality of control signals to arrange a combination selected from the first MAC unit result, the second MAC unit result, and a representation of an exceptional condition (column 6, lines 9-22).

8. Referring to claim 22, Roussel et al. have taught the method of claim 20, as described above, and wherein deferring comprises forwarding the first MAC unit result to a register (Figure 4A, element M3).

9. Referring to claim 23, Roussel et al. have taught the method of claim 20, as described above, and wherein generating comprises determining when an operand is invalid (column 6,

lines 9-22, An operand is temporarily invalid in a second Add instruction that directly follows the first.).

10. Referring to claim 24, Roussel et al. have taught the method of claim 21, as described above, and wherein generating comprises determining when an operation in combination with an operand will produce an exceptional condition (column 6, lines 9-22).

11. Referring to claim 25, Roussel et al. have taught the method of claim 20, as described above, and further comprising forwarding the combination to a result bus (Figure 4A, port 3).

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 26-30 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Worley, Jr. et al., US Patent 5,596,733.

14. Referring to claim 26, Worley, Jr. et al. have taught an apparatus comprising:

a. means for producing a plurality of control signals responsive to a first data value, a second data value, and an exceptional condition (Figure 8, control signals from elements 180, 182, 174, and 176), wherein the exception condition results from the execution of a multiply accumulate (MAC) unit over the first and second data values (abstract, column 1, lines 25-57); and

b. means for arranging a combination selected from a first MAC unit result, a second MAC unit result, and a representation of the exceptional condition

responsive to the plurality of control signals (abstract, Figure 8, Column 5, lines 22-36, A combination of result values are selected for instructions from the produced values and the default values.).

15. Referring to claim 27, Roussel et al. have taught the apparatus of claim 26, as described above, and wherein the first MAC unit result is responsive to the first data value (Figure 8). I

16. Referring to claim 28, Worley, Jr. et al. have taught the apparatus of claim 26, as described above, and wherein the second MAC unit result is responsive to the second data value (Figure 8).

17. Referring to claim 29, Worley, Jr. et al. have taught the apparatus of claim 26, as described above, and wherein the exceptional condition is identified by the MAC unit (column 1, lines 25-56, column 9, line 59-column 10, line 49, overflow and inderflow).

18. Referring to claim 30, Worley, Jr. et al. have taught the apparatus of claim 26, as described above, and wherein the exceptional condition is identified by the means for producing the plurality of control signals responsive to at least one of the first and second data values and an opcode (column 1, lines 25-56, column 9, line 59-column 10, line 49).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roussel et al., US Patent 6,230,257, cited as a prior art reference in paper number 2, mailed on September 27, 2002, in view of Worley, Jr. et al., US Patent 5,596,733.

21. Referring to claim 16, Roussel et al. have taught an apparatus comprising:

a. a Multiply accumulate (MAC) unit coupled to operand busses at respective operand inputs (Figure 4A, dashed box, column 3, lines 39-41), the MAC unit configured to latch a first multiple-bit data value during a first cycle and execute the MAC functions on the first multiple-bit data value during the next subsequent cycle while latching a second multiple-bit data value (column 4, lines 24-58, the first data value is latched into the execution unit and then the data is operated on during the subsequent cycle. The second data value is latched in M1, M2, and the execution units.), the MAC unit configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus once the first MAC result is available (column 4, lines 24-58, Figure 4A, The first Mac result is supplied on result bus, port 3, when output from M3.) and latch a second MAC result responsive to the second multiple-bit data value (column 4, lines 24-58, Figure 4A, The second MAC result is latched into the register file 400.);

b. a register coupled to the result bus and configured to latch the first MAC result (Figure 4A, element M3).

22. Roussel et al. have not specifically taught

a. a miscellaneous logic unit coupled between the result bus and the register, the miscellaneous logic unit configured to generate first and second control signals

responsive to at least one certain exceptional condition, wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus,

b. when the second control signal is asserted the first MAC result is driven from the register onto the result bus, and wherein when the second control signal s not asserted a miscellaneous-unit generated result is driven onto the result bus.

23. Worley, Jr. et al. have taught

a. a miscellaneous logic unit coupled between the result bus and the register (Figure 8, elements 174 and 176), the miscellaneous logic unit configured to generate first and second control signals responsive to at least one certain exceptional condition (column 5, lines 22-36, column 9, line 59-column 10, line 49, column 6, lines 21-60, A first control signal is generated for a first instruction and a second control signal is generated for a second instruction.), wherein when the first control signal is asserted the MAC unit supplies the second MAC result on the result bus (Figure 8, For any given instruction, when there is no exception, or the first control signal is asserted, the Function Unit A, or Mac unit, supplies the result on the result bus, element 178.),

b. when the second control signal is asserted the first MAC result is driven from the register onto the result bus, and wherein when the second control signal is not asserted a miscellaneous-unit generated result is driven onto the result bus (Figure 8, For any given instruction, when there is no exception, or the second control signal is asserted, the Function Unit A, or Mac unit, supplies the result on the result bus, element 178. When there is an exception, or the second control signal is not asserted, the storage table, element 178, result is driven onto the result bus, element 178.)

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Roussel et al. include the claimed miscellaneous logic unit, as taught by Worley, Jr. et al., for the desirable purpose of correcting exceptions that occur during runtime (Worley, Jr. et al., abstract).

25. Referring to claim 17, Roussel et al. in combination with Worley, Jr. et al. have taught the apparatus of claim 16, as described above, and wherein the miscellaneous logic unit is configured to identify an exceptional condition responsive to an operand (Worley, Jr. et al., column 1, lines 25-48).

26. Referring to claim 18, Roussel et al. in combination with Worley, Jr. et al. have taught the apparatus of claim 16, as described above, and wherein the miscellaneous logic unit is configured to recognize an exceptional condition identified by the MAC unit (Worley, Jr. et al., column 1, lines 25-48).

27. Referring to claim 19, Roussel et al. in combination with Worley, Jr. et al. have taught the apparatus of claim 18, as described above, and wherein the miscellaneous logic unit directs the replacement of one of the first and second MAC results with a representation of the exceptional condition (abstract).

Response to Arguments

28. Applicant's arguments with respect to claims 16-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER